REMARKS

REMARKS/ARGUMENTS

Claims 1-19 are pending in the application and have been rejected and have been rejected. Claims 1, 16, 17, 18, and 19 have been amended. Applicant respectfully requests reconsideration.

Rejections under 35 U.S.C. §102.

The Office Action has rejected claims 1-6 and 9-19 under 35 U.S.C. §102 as being anticipated by US Patent No. 5,898,880 issued to Ryu et al. (hereafter, "Ryu"). Applicant respectfully traverses the rejection for the following reasons.

Claim 1, as amended, requires that the memory is non-volatile and storing only strategically selected storage data in the second level of storage based on energy-conserving criteria. Ryu neither teaches nor suggests this feature. The Ryu patent addresses two issues: saving power by properly managing the disk drive state; and preventing data loss due to system power off. Ryu is exclusively concerned about the write-back cache that basically all disk drives come equipped with. He describes how this cache can be managed in such a way to reduce power consumption of the disk drive and how it can be managed to buffer some amount of data and how this buffered data can be kept in the cache for a while without risk of losing it in case of a power loss. He maintains data integrity by delaying the battery ejection, or a system power off, until the buffered data in the cache has been written to the disk. Ryu still has an inherent limitation to it, namely, the cache is volatile. Ryu would not have to delay battery ejection, or a power down, if the cache was non-volatile. Thus, Ryu may work fine as long as the OS is in control of the battery ejection, or the power down. But if someone was to yank out the battery, or if someone is operating his computer without a battery from an AC adapter and pulls the plug, then Ryu will lose the data in his cache.

The claimed invention is immune to the sudden loss of power because both levels of memory are non-volatile. The claimed invention makes it unnecessary to write our buffered data

to disk before, say, ejecting the battery. The buffered data are safe in the claimed non-volatile secondary storage and that it is a permanent storage medium. Moreover, nowhere does Ryu teach storing only strategically selected storage data in a second level storage according to energy conservation criteria.

Claims 2-15 are either directly or indirectly dependent on claim 1 and are patentable for at least the same reasons that claim 1 is patentable. Claims 16, 17, 18, and 19 have also been amended to include the non-volatile memory and the criteria for storage discussed above and are patentable for the same reasons as discussed with respect to claim 1.

Rejections under 35 U.S.C. §103.

The Office Action rejected claims 7 and 8 as unpatentable over Ryu in view of Thelander (U. S. Patent Application 2003/0009705). The Office Action concedes that Ryu does not disclose that "system stores current user profiles and the system state information comprises whether storage input/output data are associated with a current user profile." However, the Office Action contends that Thelander teaches this element and that it would have been obvious to one skilled in the art to modify Ryu according to Thelander such that the limitations of claim 7 are met. The motivation cited for making the combination is that "doing so would have been to have a, 'power saving apparatus for hard disk drive, which enables disk cache to operate in a write back mode, so that it restricts had disk drive access as much as possible, without having lost the data in the cache when a sudden system power off has occurred.'" This is a misquote of the cited part of Ryu which actually reads: "power saving apparatus constructed according to the principles of the present invention. The power saving apparatus is configured to control hard disk drive by using a write back mode disk cache that reduces the number of time in which the hard disk drive is accessed in order to reduce the power consumption of battery by the hard disk drive. Usually, the write back mode allows the disk cache to operate such that once data contained in the cache has changed, the changed data remains in the cache and the data may not be written onto the hard disk. Meanwhile, if such data is not found in the cache, that is, the miss hit occurs,

then all the changed data is written on the hard disk media while an access to the hard disk is performed to find necessary data." Applicant respectfully submits that claims 7 or 8 would not have been obvious in view of the combination of Ryu and Thelander. The concept of storing only strategically selected information is not taught or suggested in the references. In RYU once the CPU is in a write back mode, all information is stored in the cache. Thelander contains no teaching or motivation to modify Ryu as suggested by the examiner.

Claim 11 has been rejected under 35 USC §103 as being obvious over Ryu in view of Applicant's admitted prior art. The Office Action concedes that Ryu does not disclose on the use of Flash memory for the second levels of storage hierarchy. Claim 11 is dependent on claim 1 and is patentable for the same reasons as claim 1. Applicant has not admitted that the claimed combination is old. The statement made in the Background is "These media *could be* alternate non-volatile memory such as Flash memory, ...(emphasis added)". That is a statement of possible solutions not an admission that those devices exist.

For the foregoing reasons, Applicant respectfully requests allowance of the pending claims and that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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I hereby certify that this Preliminary Amendment, and any documents referred to as attached therein, are being deposited in the U. S. Post Office as first-class mail on this date, January 23, 2006, to the Commissioner for Patents, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450, this 10th day of April, 2006.

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